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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,351	04/15/2004	Lindsey H. Hall	TI-35168	8635

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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/825,351	HALL ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 16-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/15/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 1-10 and 16-20, in the reply filed on July 11, 2005 is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5, a dependent claim of claim 1, recites the limitation "said gas compound" in the first sentence of the claim. As the gas compound is only referenced in claim 4, there is insufficient antecedent basis for this limitation in either claim 1 or claim 5.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3, 9-10, 16 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Nagano et al. '327.

Nagano et al. discloses a method of fabricating an integrated circuit and a method of reducing recess relief within an interconnect structure located in a layer of a semiconductor device comprising forming transistors on a semiconductor substrate, depositing dielectric layers over the transistors, forming an interconnect structure located in the dielectric layer, and forming a metal-insulator-metal capacitor on the interconnect structure (col. 3, lines 36-50). The reference further discloses the method to include conducting a fabrication process on the interconnect that recesses the interconnect and forms a recessed dielectric layer (col. 6, lines 46-67), and subsequently conducting a recess reduction etch to remove a portion of the recessed dielectric layer to reduce a relief of the recessed dielectric layer and form a substantially planar surface about the interconnect structure prior to forming the metal-insulator-metal capacitor (col. 7, lines 3-18). The references also discloses the recess reduction etch being performed under non-oxidizing conditions (col. 7, lines 9-15), and the etch resulting in a recess depth of zero nanometers (col. 10, lines 9-13).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4, 6-7, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano et al. '327 as described above, and further in view of Dubin et al. '190.

Nagano et al. discloses all of the elements of claims 1 and 16, and also teaches the use of an argon gas dry etch to perform the recess reduction etch (col. 7, lines 3-5). Nagano does not teach the dry etch gas mixture of the fluorinated hydrocarbon compound CH2F2, nitrogen or hydrogen, and argon gas. Dubin et al. teaches the use of CH2F2, argon, and nitrogen to etch dielectric layers in the formation of an interconnect (¶18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the etch gas mixture of Dubin et al. in the interconnect process of Nagano et al. because the mixture of fluorinated hydrocarbons, nitrogen, and argon is functionally equivalent for dielectric etching, and the mixture can be tailored to the etch rates of various dielectric materials.

8. Insofar as definite, claims 5, 8, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagano et al. in view of Dubin et al. as described above, and further in view of Chen '003.

Nagano et al. discloses all of the elements of claims 1 and 16, but fails to teach the use of a fluorinated hydrocarbon flowing at about 20 sccm, argon flowing at about 100 sccm, and nitrogen or hydrogen flowing at about 100 sccm. Nagano et al. also fails to disclose the etch duration time. Chen teaches a method of forming an interconnect and metal-insulator-metal capacitor that uses a fluorinated hydrocarbon at a flow rate of about 20 sccm and uses inert gases at of flow of about 100 sccm (col. 9, lines 12-16). The reference also discloses performing a dielectric layer etch for about 10 seconds (col. 9, lines 3-7). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the claimed etch flow rates and etch time in the method of Nagano et al. because Chen teaches that the use of these flow rates and etch time for this application was known, and evidence that the selection of the specified flow rates and etch time would have merely constituted an obvious optimization determinable through routine experimentation in order to tailor the dielectric etch to the desired etch rate and dielectric layer profile.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Seo et al. '022 discloses a method of making a metal-insulator-metal capacitor over an interconnect wherein the interconnect is

formed by depositing a metal layer over a via-hole in a dielectric, the metal layer removed by dry etching, and the dielectric then is dry etched to allow the interconnect to protrude from the surface of the dielectric.

b. Harris et al. '044 discloses a method of making a metal-insulator-metal capacitor over an interconnect wherein the bottom electrode of the capacitor is formed out of several metal layers, thus filling any defects at the interconnect-capacitor interface.

c. Ference et al. '775 discloses a method of making a planar interconnect by depositing a metal layer over a via-hole in dielectric, chemical-mechanical polishing the metal down to a thin layer over the via, and dry etching the remaining metal layer down to the surface of the dielectric.

d. Uchiyama et al. '920 discloses a method of making planar interconnect by depositing a metal layer over a via-hole in a dielectric, then performing a two step dry etch to remove the metal layer down to the surface of the dielectric.

e. Chen '067 and Sato '787 disclose a method of making planar interconnect by depositing a metal layer over a via-hole in a dielectric, performing a dry etch to remove the majority of the metal layer down

to the surface of the dielectric, and performing a chemical-mechanical polish to planarize the surface of the interconnect to the dielectric.

f. Modak '710, Yu et al. '534, and Liu et al. '078 disclose a method of making planar interconnect by depositing a metal layer over a via-hole in a dielectric and performing a two step chemical-mechanical polish to remove the metal layer down to the surface of the dielectric.

g. Sun et al. '837 discloses a method of making a planar interconnect by depositing a layer of dielectric over a patterned metal layer and dry etching the dielectric down to the surface of the metal.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sjf
8/2/05

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER